REMARKS/ARGUMENTS

In the Office Action mailed February 27, 2009, claims 1-20 were rejected. In response, Applicants hereby request reconsideration of the application in view of the below-provided remarks. No claims are amended, added, or canceled.

Claim Rejections under 35 U.S.C. 102 and 103

Claims 1, 2, 4, 5, 7, 8, 13, 14, and 17 were rejected under 35 U.S.C. 102(b) as being anticipated by Cherabuddi (U.S. Pat. No. 6,725,336, hereinafter Cherabuddi). Additionally, claims 3, 9-11, and 18 were rejected under 35 U.S.C. 103(a) as being unpatentable over Cherabuddi in view of Asher et al. (U.S. Pat. No. 6,671,822, hereinafter Asher). Additionally, claim 6 was rejected under 35 U.S.C. 103(a) as being unpatentable over Cherabuddi in view of Kramer (U.S. Pat. No. 4,868,869, hereinafter Kramer). Additionally, claim 12 was rejected under 35 U.S.C. 103(a) as being unpatentable over Cherabuddi in view of Supnik (U.S. Pat. No. 5,070,502, hereinafter Supnik). Additionally, claim 15 was rejected under 35 U.S.C. 103(a) as being unpatentable over Cherabuddi in view of Emma et al. (U.S. Pat. No. 5,584,002, hereinafter Emma). However, Applicants respectfully submit that these claims are patentable over Cherabuddi, Asher, Kramer, Supnik, and Emma for the reasons provided below.

Independent Claim 1

Claim 1 recites "remapping means (RM, MapRAM) for performing an unrestricted remapping within said plurality of memory modules, wherein the unrestricted remapping permits remapping the memory modules from a first physical bank of memory modules to a second physical bank of memory modules" (emphasis added).

In contrast, Cherabuddi does not disclose all of the limitations of the claim because Cherabuddi does not disclose remapping memory modules from a first physical bank of memory modules to a second physical bank of memory modules, as recited in the claim. In fact, the Office Action recognizes that Cherabuddi does not explicitly disclose

the indicated limitation. The Office Action recognizes this lack of explicit disclosure by Cherabuddi because the Office Action asserts that it is allegedly inherent in Cherabuddi to remap memory modules between first and physical banks. However, this assertion of inherency is insufficient to support the rejection of claim 1 at least because the assertion of inherency is not properly supported by rationale or evidence, as required by the MPEP.

The MPEP states that the Examiner must provide rationale or evidence in order to show inherency. MPEP 2112(IV). More specifically, in relying on a theory of inherency, the Examiner must provide a basis in fact and/or technical reasoning to reasonably support the assertion that an allegedly inherent characteristic necessarily flows from the teachings of the cited reference. Id. Moreover, the MPEP states that the possible occurrence of a result or characteristic is not sufficient to establish inherency of the asserted result or characteristic. Id.

The conclusion of inherency asserted in the Office Action is not supported by any rationale or evidence. Here, the Office Action merely restates some of the disclosure of Cherabuddi related to allocating different cache memory partitions to different active processors. In general, Cherabuddi describes a multiprocessor computer system which includes multiple processors and a shared cache memory. Cherabuddi, abstract. The cache memory is partitioned into first and second cache memory partitions. Cherabuddi, col. 3, lines 31-34. A cache access circuit dynamically allocates the cache resources (i.e., the first and second cache memory partitions) between the first and second processors according to each processor's processing requirements. Cherabuddi, col. 3, lines 42-46. For example, if both processors are active, then the cache access circuit allows each processor to use a corresponding cache memory partition as dedicated cache. Cherabuddi, col. 2, lines 7-12. As another example, if only one processor is active, then the cache access circuit allows the active processor to use both the first and second cache memory partitions. Cherabuddi, col. 2, lines 25-29. Thus, Cherabuddi merely describes allocating cache memory partitions between multiple processors. However, Cherabuddi does not address remapping memory modules between different physical banks of memory.

Although the Office Action concludes that remapping memory modules between different physical banks of memory is allegedly inherent, based on the description of dynamically allocating different cache memory partitions to different active processors, the Office Action does not attempt to provide any rationale to explain why or how remapping memory modules between different physical banks of memory might be inherent. More specifically, the Office Action does not attempt to explain how the disclosure of allocating different cache memory partitions to different processors (or to the same processor), generally, might lead to the asserted conclusion of inherency regarding remapping memory modules between different physical banks of memory. Additionally, the Office Action does not describe any facts or technical reasoning that would support the assertion of inherency. Moreover, the Office Action does not provide any extrinsic evidence to remedy this lack of rationale. In other words, the Office Action asserts the unsupported conclusion of inherency, without providing any rationale or evidence to show how the Examiner might have arrived at the asserted conclusion of inherency.

Therefore, the rejection of claim 1 based on the asserted disclosure of Cherabuddi is improper because the assertion of inherency is not properly supported by rationale or evidence as required by the MPEP. Accordingly, Applicants respectfully submit claim 1 is patentable over Cherabuddi because Cherabuddi does not disclose all of the limitations of the claim.

Independent Claim 8

Applicants respectfully assert independent claim 8 is patentable over Cherabuddi at least for similar reasons to those stated above in regard to the rejections of independent claim 1. In particular, claim 8 recites "performing an unrestricted remapping within said plurality of memory modules, wherein the unrestricted remapping permits remapping the memory modules from a first physical bank of memory modules to a second physical bank of memory modules" (emphasis added).

Here, although the language of claim 8 differs from the language of claim 1, and the scope of claim 8 should be interpreted independently of claim 1, Applicants respectfully assert that the remarks provided above in regard to the rejections of claim 1

also apply to the rejections of claim 8. Accordingly, Applicants respectfully assert claim 8 is patentable over Cherabuddi because Cherabuddi does not disclose remapping memory modules between physical banks of memory modules within a cache memory, as recited in the claim.

Dependent Claims

Claims 2-7 and 9-20 depend from and incorporate all of the limitations of the corresponding independent claims 1 and 8. Applicants respectfully assert claims 2-7 and 9-20 are allowable based on allowable base claims. Additionally, each of claims 2-7 and 9-20 may be allowable for further reasons, as discussed below.

In regard to the rejection of claim 9, Applicants submit that the rejection of claim 9 is improper because Cherabuddi does not disclose all of the limitations of the claims. The Office Action relies on Cherabuddi as purportedly disclosing an SC bit which acts as a lookup table for a faulty module. In particular, the Office Action states that the SC bit is disclosed in Cherabuddi at col. 9, lines 9-11. However, Cherabuddi does not disclose an SC bit at the indicated location or at any other location of the disclosure. Therefore, the rejection of claim 9 based on the disclosure of Cherabuddi is improper because the actual disclosure of Cherabuddi does not support the assertions presented in the Office Action under 35 U.S.C. 102.

In regard to the rejections of claims 13 and 17, Applicants submit that these claims are patentable over Cherabuddi because Cherabuddi does not disclose all of the limitations of the claims. Claim 13 recites "the remapping means is further configured to remap at least one of the memory modules to a new way and a same index within the second physical bank of memory modules." Claim 17 recites similar limitations. Rather than show how Cherabuddi might disclose these limitations, the Office Action merely concludes that the disclosure of Cherabuddi inherently discloses these limitations. However, the conclusion of inherency asserted in the Office Action is not supported by any rationale or evidence. The Office Action merely states that Cherabuddi describes combining 2-way set associative caches to form a 4-way set associative cache, but the Office Action does not attempt to explain how forming a 4-way set associative cache in this manner might inherently disclose remapping memory modules to a new way.

Therefore, the rejection of the claims based on the asserted disclosure of Cherabuddi is improper because the assertion of inherency is not properly supported by rationale or evidence as required by the MPEP. Accordingly, Applicants respectfully submit claims 13 and 17 are patentable over Cherabuddi because Cherabuddi does not disclose all of the limitations of the claims. Furthermore, even if the disclosure of Cherabuddi were to inherently disclose remapping memory modules to a new way, the Office Action nevertheless fails to assert or address remapping to a new way and a same index, as recited in the claim. Thus, the Office Action's assertions of inherency also fail to address the language of the claim, as a whole.

In regard to the rejections of claims 11 and 18, Applicants submit that the claims are patentable over the combination of Cherabuddi and Asher because the combination of cited references does not teach all of the limitations of the claims. Claim 11 recites "the remapping means is further configured to remap at least one of the memory modules from an index within the first physical bank of memory modules to a new way and a different index within the second physical bank of memory modules." Claim 18 recites similar limitations. Rather than show how the combination of cited references might teach remapping memory modules to a new way, the Office Action merely concludes that the disclosure of Cherabuddi inherently teaches remapping memory modules to a new way, as explained above with references to the rejections of claims 13 and 17. However, the conclusion of inherency asserted in the Office Action is not supported by any rationale or evidence. The Office Action merely states that Cherabuddi describes combining 2-way set associative caches to form a 4-way set associative cache, but the Office Action does not attempt to explain how forming a 4-way set associative cache in this manner might inherently teach remapping memory modules to a new way. Therefore, the rejection of the claims based on the asserted teachings of Cherabuddi is improper because the assertion of inherency is not properly supported by rationale or evidence as required by the MPEP. Accordingly, Applicants respectfully submit claims 11 and 18 are patentable over the combination of Cherabuddi and Asher because the combination of cited references does not teach all of the limitations of the claims.

CONCLUSION

Applicants respectfully request reconsideration of the claims in view of the remarks made herein. A notice of allowance is earnestly solicited.

At any time during the pendency of this application, please charge any fees required or credit any over payment to Deposit Account **50-4019** pursuant to 37 C.F.R. 1.25. Additionally, please charge any fees to Deposit Account **50-4019** under 37 C.F.R. 1.16, 1.17, 1.19, 1.20 and 1.21.

Respectfully submitted,

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